

## CLAIMS

1. A precedence determination system, comprising:
  - a first type memory bank configured to receive a first search signal and to provide a plurality of first search result indications;
  - a second type memory bank configured to receive a second search signal and to provide a plurality of second search result indications;
  - a precedence number table coupled to the first and second type memory banks and configured to provide a plurality of programmable precedence numbers; and
  - a precedence determination circuit coupled to the first and second type memory banks and the precedence number table and configured to provide a third search result indication.
2. The precedence determination system of claim 1, wherein:
  - the first type memory bank includes static random access memory (SRAM).
3. The precedence determination system of claim 1, wherein:
  - the second type memory bank includes ternary content addressable memory (TCAM).
4. The precedence determination system of claim 2, wherein:
  - the first type memory bank includes a plurality of entries.
5. The precedence determination system of claim 3, wherein:
  - the first type memory bank includes a plurality of entries.
6. The precedence determination system of claim 1, wherein:
  - the first search signal includes a hash function signal.
7. The precedence determination system of claim 1, wherein:
  - the second search signal includes a search key.
8. The precedence determination system of claim 4, wherein:
  - each of the plurality of entries is configured to select one of the plurality of programmable precedence numbers.
9. The precedence determination system of claim 5, wherein:

each of the plurality of entries is configured to select one of the plurality of programmable precedence numbers.

10. The precedence determination system of claim 6, wherein:  
each of the plurality of first search result indications includes a hit or miss indication in response to the hash function signal.
11. The precedence determination system of claim 7, wherein:  
each of the plurality of second search result indications includes at most one hit indication in response to the search key.
12. The precedence determination system of claim 11, wherein:  
the at most one hit indication is provided in response to a physical address based precedence.
13. The precedence determination system of claim 1, wherein:  
the third search result indication includes an overall hit or miss indication.
14. The precedence determination system of claim 13, wherein:  
the overall miss indication includes a default precedence value.
15. A method of determining a precedence, comprising the steps of:  
searching a first type memory to provide a plurality of first search results;  
searching a second type memory to provide a plurality of second search results;  
selecting a plurality of precedence numbers from a precedence number table in response to the first and second search results;  
determining a precedence in response to the plurality of precedence numbers; and  
providing a third search result.
16. The method of determining the precedence of claim 15, wherein:  
the first type memory includes static random access memory (SRAM).
17. The method of determining the precedence of claim 15, wherein:  
the second type memory includes ternary content addressable memory (TCAM).

18. The method of determining the precedence of claim 15, wherein:  
the steps of searching the first type memory and searching the second type memory are performed substantially in parallel.
19. The method of determining the precedence of claim 15, wherein:  
the third search result includes an overall hit or miss indication.
20. The method of determining the precedence of claim 19, wherein:  
the overall miss indication includes a default precedence value.
21. The method of determining the precedence of claim 15, wherein:  
the plurality of precedence numbers are programmable.
22. A means for determining a precedence, comprising:  
a means for searching a first type memory to provide a plurality of first search results;  
a means for searching a second type memory to provide a plurality of second search results;  
a means for selecting a plurality of precedence numbers from a precedence number table in response to the first and second search results;  
a means for determining a precedence in response to the plurality of precedence numbers;  
and  
a means for providing a third search result.